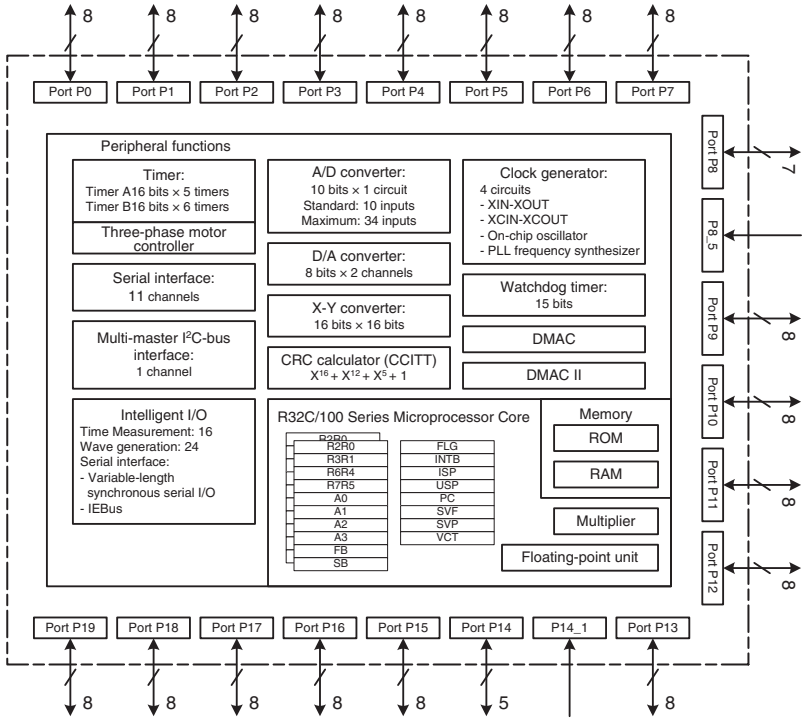
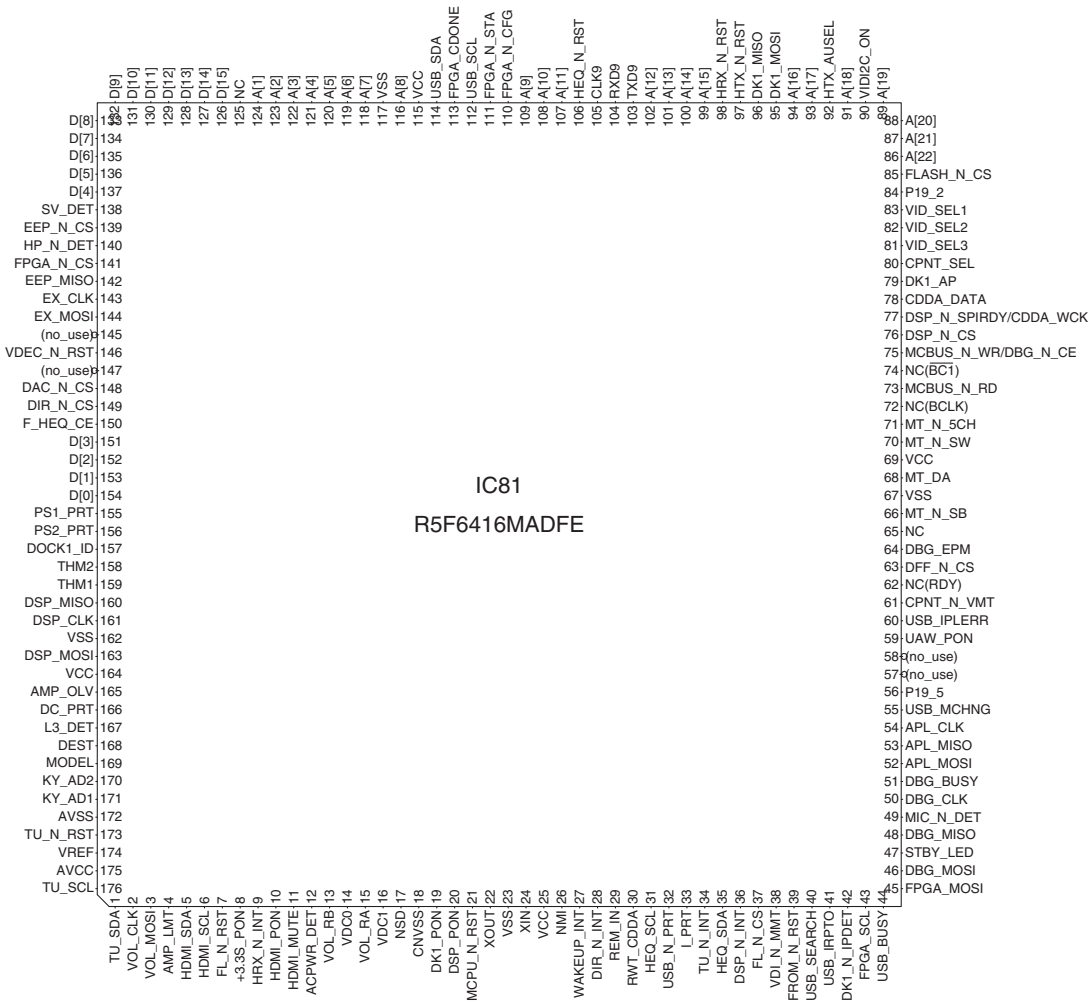
■ IC DATA

IC81: R5F6416MADFE (DIGITAL1 P.C.B.)
Microprocessor

*** No replacement part available. / サービス部品供給なし**





Pin No.	Port Name	Function Name	Related Power Supply				Detail of Function
			ON		OFF		
			I/O	Logic	I/O	Logic	
1	SRXD4/SDA4/TXD4/ ANEX1/P9_6	TUN_SDA	I/O	Data	O	Low	Tuner I2C data
2	CLK4/ANEX0/P9_5	HDR_MOSI	O	Data	O	Low	HD Radio transmission data (U model)
		VOL1_SCK	O	Clock	O	Low	VOL1 (R2A15220FP #1) communication clock
3	N_CTS4/N_N_RTS4/ N_SS4/TB4IN/DA1/ P9_4	VOL_MOSI	O	Data	O	Low	VOL1/VOL2/VOL3 communication data
4	N_CTS3/N_N_RTS3/ N_SS3/TB3IN/DA0/ P9_3	AMP_LMT	O	D/A	I	---	Limiter control
5	IEOUT/ISTXD2/ OUTC2_0/SRXD3/ SDA3/TXD3/TB2IN/ P9_2	HDMI_SDA	I/O	Data	O	Low	HDMI and DVIDEO(AVIDEO:Vx071) 400k I2C data
6	IEIN/ISRXD2/STXD3/ SCL3/RXD3/TB1IN/ P9_1	HDMI_SCL	O	Clock	O	Low	HDMI and DVIDEO (AVIDEO:Vx071) 400k I2C clock
7	CLK3/TB0IN/P9_0	VOL2_SCK	O	Clock	O	Low	VOL2 (R2A15220FP #2) communication clock
8	P19_7	VOL3_SCK	O	Clock	O	Low	VOL3 (NJW1194V, NJU7313AM) communication clock
9	N_INT8/P14_6	HRX_N_INT	I	L act	O	Low	Interrupt from HDMI RX
10	P19_6	FLD_N_RST	O	L act	O	Low	FLD reset
11	N_INT7/P14_5	HDMI_MUTE	I	H act	O	Low	Mute from HDMI RX
12	N_INT6/P14_4	PWR_DET	I	L act	I	---	AC power detect
13	P14_3	FLD_N_CS	O	L act	O	Low	FLD chip select
14	VDC0	VDC0					---
15	P14_1 (for exclusive use of the input)	I_PRT	I	H act	I	---	Current protection
16	VDC1	VDC1					---
17	NSD	NSD					Debugger
18	CNVSS	DBG_CNVSS					---
19	XCIN/P8_7	MIC_N_DET	I	L act	O	Low	Microphone detection
20	XCOUT/P8_6	PD_LED	O	H act	O	Low	PURE DIRECT LED
21	RESET	MCPU_N_RST					---
22	XOUT	XOUT					---
23	VSS	VSS					---
24	XIN	XIN					---
25	VCC	VCC					---
26	NMI/P8_5	NMI					---
27	N_INT2/P8_4	WAKEUP_INT	I	Both edges	O	Low	Power switch, MISO interrupt of RS-232C and Dock (Sleep return)
28	N_INT1/P8_3	REM_IN2	I	L act	O	Low	Remote control pulse input 2
29	N_INT0/P8_2	REM_IN1	I	L act	O	Low	Remote control pulse input 1
30	UD0B/UD1B/IIO1_5/ N_RTS5/N_CTS5/N_ SS5/U/TA4IN/P8_1	TUN_N_INT	I	L act	O	Low	Interrupt from TUNER
		---	O	Low	O	Low	No used
31	UD0A/UD1A/RXD5/ SCL5/STXD5/U/ TA4OUT/P8_0	HEQ_SCL	O	Clock	O	Low	HDMI switcher 100k I2C clock
32	P18_1	FLD_PON	O	H act	O	Low	FL driver +3.3V power supply control
33	P18_0	STBY_LED	O	H act	O	Low	Standby LED control
34	UD0B/UD1B/IIO1_4/ CLK5/TA3IN/P7_7	DSP1_N_INT	I	L act	O	Low	Interrupt from DSP1
35	UD0A/UD1A/IIO1_3/ N_RTS8/N_CTS8/ TXD5/SDA5/SRXD5/ TA3OUT/P7_6	HEQ_SDA	I/O	Data	O	Low	HDMI switcher 100k I2C data
36	IIO1_2/RXD8/W/ TA2IN/P7_5	DIR_N_INT	I	L act	O	Low	Interrupt from DIR
37	IIO1_1/CLK8/W/ TA2OUT/P7_4	IR_CAR	O	Data	O	Low	Carrier output for SCENE IR (spare)
38	P17_7	ISEL_RA	I		I	---	Input selector A
39	P17_6	ISEL_RB	I		I	---	Input selector B
40	P17_5	VOL_RA	I		I	---	Volume A
41	P17_4	VOL_RB	I		I	---	Volume B

Pin No.	Port Name	Function Name	Related Power Supply				Detail of Function
			ON		OFF		
			I/O	Logic	I/O	Logic	
42	IIO1_0/TXD8/N_SS2/ N_RTS2/N_CTS2/V/ TA1IN/P7_3	DK1_N_IPDET	I	L act	O	Low	Dock iPod detect
43	CLK2/V/TA1OUT/ P7_2	SR_PON	O	H act	O	Low	SIRIUS power supply control
44	MSCL/IEIN/ISRXD2/ OUTC2_2/IIO1_7/ STXD2/SCL2/RXD2/ TA0IN/TB5IN/P7_1	SR_MISO	I	Data	O	Low	SIRIUS reception data
45	TA0OUT/TXD2/ SDA2/SRXD2/ IIO1_6/OUTC2_0/ ISTXD2/IEOUT/ MSDA/P7_0	SR_MOSI	O	Data	O	Low	SIRIUS transmission data
46	TXD1/SDA1/SRXD1/ P6_7	232C_DBG_MOSI	O	Data	O	Low	RS-232C transmission data / Debug / E8a
47	P14_7	DSP_PON	O	H act	O	Low	DSP power supply
48	RXD1/SCL1/STXD1/ P6_6	232C_DBG_MISO	I	Data	O	Low	RS-232C reception data / Debug / E8a
49	P11_7	DAC_N_CS	O	L act	O	Low	DAC chip select (SW of V3071, FP DAC is D-FF)
50	CLK1/P6_5	DBG_SCK	I	Clock	O	Low	E8a
51	N_CTS1/N_RTS1/ N_SS1/OUTC2_1/ ISCLK2/P6_4	DBG_BUSY	O		O	Low	E8a
52	TXD0/SDA0/SRXD0/ P6_3	DSP_MOSI	O	Data	O	Low	DSP/DIR/DAC transmission data
53	TB2IN/RXD0/SCL0/ STXD0/P6_2	DSP_MISO	I	Data	I	---	DSP/DIR/DAC reception data
54	TB1IN/CLK0/P6_1	DSP_SCK	O	Clock	O	Low	DSP/DIR/DAC communication clock
55	TB0IN/N_CTS0/N_ RTS0/N_SS0/P6_0	NCPU_N_INT	I	H act	O	Low	Network microprocessor interrupt
56	P19_5	ADC_N_RST	O	L act	O	Low	ADC reset (power down)
57	D31/OUTC2_7/ P13_7	DSP1_N_RST	O	L act	O	Low	DSP1 reset
58	D30/OUTC2_1/ ISCLK2/P13_6	EX_SCK	O	Clock	O	Low	FL/EEPROM/ expansion IO communication clock
59	D29/OUTC2_2/IS- RXD2/IEIN/P13_5	EEP_MISO	I	Data	O	Low	EEPROM reception data
60	D28/OUTC2_0/ ISTXD2/IEOUT/ P13_4	EX_MOSI	O	Data	O	Low	FL/EEPROM/ expansion IO transmission data
61	P19_4	EEP_N_CS	O	L act	O	Low	EEPROM chip select
62	RDY/CS3/N_CTS7/ N_RTS7/P5_7	FPGA_N_CS	B	Bus	O	Low	External bus FPGA chip select
63	ALE/CS2/RXD7/P5_6	DFF2_N_CS	B	Bus	O	Low	External bus DFF2 chip select
64	HOLD/CLK7/P5_5	DBG_EPM	I		I	---	E8a
65	HLDA/CS1/TXD7/ P5_4	DFF1_N_CS	B	Bus	O	Low	External bus DFF1 chip select
66	D27/OUTC2_3/ P13_3	DSP2_N_SPIRDY	I	L act	O	Low	DSP2 SPI ready
67	VSS	VSS					---
68	D26/OUTC2_6/ P13_2	DSP1_N_SPIRDY	I	L act	O	Low	DSP1 SPI ready
69	VCC	VCC					---
70	D25/OUTC2_5/ P13_1	DSP2_N_CS	O	L act	O	Low	DSP2 chip select
71	D24/OUTC2_4/ P13_0	DSP1_N_CS	O	L act	O	Low	DSP1 chip select
72	CLKOUT/BCLK/P5_3	NC(BCLK)	B	Bus	O	Low	External bus
73	RD/P5_2	MCBUS_N_RD	B	Bus	O	Low	External bus
74	WR1/BC1/P5_1	NC(BC1)	B	Bus	O	Low	External bus
75	WR0/WR/P5_0	MCBUS_N_WR	B	Bus	I	---	External bus
		DBG_N_CE	I		I	---	E8a
76	D23/P12_7	MT_DA	O	H act	O	Low	Mute Digital Audio
77	D22/P12_6	DIR_N_CS	O	L act	O	Low	DIR chip select
78	D21/P12_5	DIR_N_RST	O	L act	O	Low	DIR reset

Pin No.	Port Name	Function Name	Related Power Supply				Detail of Function
			ON		OFF		
			I/O	Logic	I/O	Logic	
79	P19_3	DK1_AP	I	L act	I	---	iPod accessory power
80	P17_3	DK1_PON	O	H act	O	Low	Dock power supply
81	P17_2	UAW_PON	O	H act	O	Low	UAW power supply control
82	P17_1	NCPU_PON	O	H act	O	Low	NET/USB power supply
83	P17_0	NET_SEL_M	O	H NET	O	Low	Main USB/NET select
84	P19_2	NET_SEL_Z	O	H NET	O	Low	Zone USB/NET select
85	CS0/A23/TXD6/ SDA6/SRXD6/P4_7	FLASH_N_CS	O	L act	O	Low	External bus Flash ROM chip select
86	CS1/A22/RXD6/ SCL6/STXD6/P4_6	A[22]	B	Bus	O	Low	External bus
87	CS2/A21/CLK6/P4_5	A[21]	B	Bus	O	Low	External bus
88	CS3/A20/N_CTS6/N_ RTS6/N_SS6/P4_4	A[20]	B	Bus	O	Low	External bus
89	A19/TXD3/SDA3/ SRXD3/OUTC2_0/ ISTXD2/IEOUT/P4_3	A[19]	B	Bus	O	Low	External bus
90	P11_6	---	O	Low	O	Low	Spare
91	A18/RXD3/SCL3/ STXD3/ISRXD2/IEIN/ P4_2	A[18]	B	Bus	O	Low	External bus
92	P11_5	---	O	Low	O	Low	Spare
93	A17/CLK3/P4_1	A[17]	B	Bus	O	Low	External bus
94	A16/N_CTS3/N_ RTS3/N_SS3/P4_0	A[16]	B	Bus	O	Low	External bus
95	P16_7/TXD10	DK_MOSI	O	Data	O	Low	Dock UART transmission data
96	P16_6/RXD10	DK_MISO	I	Data	I	---	Dock UART reception data (3.3V logic input)
97	P16_5/CLK10	R32C_N_INT	O	L act	O	Low	Interrupt of R32C to Blackfin
98	P16_4/N_CTS10/N_ RTS10	BF_MT	I	H act	O	Low	Mute signal from Blackfin (NCPU_N_INT distinction use)
99	A15/[A15/D15]/TA4IN/ U/P3_7	A[15]	B	Bus	O	Low	External bus
100	A14/[A14/D14]/ TA4OUT/U/P3_6	A[14]	B	Bus	O	Low	External bus
101	A13/[A13/D13]/TA2IN/ W/P3_5	A[13]	B	Bus	O	Low	External bus
102	A12/[A12/D12]/ TA2OUT/W/P3_4	A[12]	B	Bus	O	Low	External bus
103	P16_3/TXD9	NCPU_PIC_MISO	O	Data	O	Low	Network microprocessor SPI transmission data
104	P16_2/RXD9	NCPU_PIC_MOSI	I	Data	O	Low	Network microprocessor SPI reception data
105	P16_1/CLK9	NCPU_PIC_SCK	I	Clock	O	Low	Network microprocessor SPI communication clock
106	P16_0/N_CTS9/N_ RTS9	NCPU_N_RST	O	L act	O	Low	Network microprocessor reset
107	A11/[A11/D11]/TA1IN/ V/P3_3	A[11]	B	Bus	O	Low	External bus
108	A10/[A10/D10]/ TA1OUT/V/P3_2	A[10]	B	Bus	O	Low	External bus
109	A9/[A9/D9]/TA3OUT/ UD0B/UD1B/P3_1	A[9]	B	Bus	O	Low	External bus
110	D20/P12_4	---	O	Low	O	Low	Spare
111	D19/N_CTS6/N_ RTS6/N_SS6/P12_3	---	O	Low	O	Low	Spare
112	D18/RXD6/SCL6/ STXD6/P12_2	---	O	Low	O	Low	Spare (After FPGA Config, I2C is possible)
113	D17/CLK6/P12_1	FPGA_SCK	O	Clock	O	Low	FPGA clock (at Boot)
114	D16/TXD6/SDA6/ SRXD6/P12_0	FPGA_MOSI	O	Data	O	Low	FPGA transmission data (at Boot)
115	VCC	VCC					---
116	A8/[A8/D8]/TA0OUT/ UD0A/UD1A/P3_0	A[8]	B	Bus	O	Low	External bus
117	VSS	VSS					---
118	A7/[A7/D7]/AN2_7/ P2_7/TXD10	A[7]	B	Bus	O	Low	External bus
119	A6/[A6/D6]/AN2_6/ P2_6/RXD10	A[6]	B	Bus	O	Low	External bus
120	A5/[A5/D5]/AN2_5/ P2_5/CLK10	A[5]	B	Bus	O	Low	External bus

Pin No.	Port Name	Function Name	Related Power Supply				Detail of Function
			ON		OFF		
			I/O	Logic	I/O	Logic	
121	A4/[A4/D4]/AN2_4/ P2_4/N_CTS10/N_ RTS10	A[4]	B	Bus	O	Low	External bus
122	A3/[A3/D3]/AN2_3/ P2_3/TXD9	A[3]	B	Bus	O	Low	External bus
123	A2/[A2/D2]/AN2_2/ P2_2/RXD9	A[2]	B	Bus	O	Low	External bus
124	A1/[A1/D1]/BC2/ [BC2/D1]/AN2_1/ P2_1/CLK9	A[1]	B	Bus	O	Low	External bus
125	A0/[A0/D0]/BC0/ [BC0/D0]/AN2_0/ P2_0/N_CTS9/N_ RTS9	A[0]	B	Bus	O	Low	External bus
126	D15/N_INT5/IIO0_7/ IIO1_7/P1_7	D[15]	B	Bus	I	---	External bus
127	D14/N_INT4/IIO0_6/ IIO1_6/P1_6	D[14]	B	Bus	I	---	External bus
128	D13/N_INT3/IIO0_5/ IIO1_5/P1_5	D[13]	B	Bus	I	---	External bus
129	D12/IIO0_4/IIO1_4/ P1_4	D[12]	B	Bus	I	---	External bus
130	D11/IIO0_3/IIO1_3/ P1_3	D[11]	B	Bus	I	---	External bus
131	D10/IIO0_2/IIO1_2/ P1_2	D[10]	B	Bus	I	---	External bus
132	D9/IIO0_1/IIO1_1/ P1_1	D[9]	B	Bus	I	---	External bus
133	IIO0_0/IIO1_0/D8/ P1_0	D[8]	B	Bus	I	---	External bus
134	AN0_7/D7/P0_7	D[7]	B	Bus	I	---	External bus
135	AN0_6/D6/P0_6	D[6]	B	Bus	I	---	External bus
136	AN0_5/D5/P0_5	D[5]	B	Bus	I	---	External bus
137	AN0_4/D4/P0_4	D[4]	B	Bus	I	---	External bus
138	P19_1	FPGA_N_CFG	O	L act	O	Low	FPGA nCONF
139	WR3/BC3/P11_4	FPGA_N_STA	I	L act	I	---	FPGA nSTATUS
140	P19_0	FPGA_CDONE	I	H act	I	---	FPGA CONF DONE
141	IIO1_3/N_RTS8/N_ CTS8/WR2/CS3/ P11_3	SCR_N_INT	I	L act	I	---	Interrupt of scaler
142	IIO1_2/RXD8/CS2/ P11_2	NCPU_MISO	I	Data	O	Low	Network microprocessor UART reception data
143	IIO1_1/CLK8/CS1/ P11_1	MT_N_Z3	O	L act	O	Low	Mute Zone3/Rear Presence (Preout)
144	IIO1_0/TXD8/CS0/ P11_0	NCPU_MOSI	O	Data	O	Low	Network microprocessor UART transmission data
145	P18_7	MT_N_F_MI	O	L act	O	Low	Mute Front (Main amplifier input)
146	P18_6	MT_N_Z2	O	L act	O	Low	Mute Zone2/Front Presence (Preout)
147	P18_5	MT_N_SB_PO	O	L act	O	Low	Mute SB (Preout)
148	P18_4	MT_N_MZ	O	L act	O	Low	Mute Main Zone (Preout/Main amplifier input)
149	P18_3	MT_N_EX1_MI	O	L act	O	Low	Mute SP1 (Main amplifier input)
150	P18_2	MT_N_SB_MI	O	L act	O	Low	Mute Surround back (Main amplifier input)
151	AN0_3/D3/P0_3	D[3]	B	Bus	I	---	External bus
152	AN0_2/D2/P0_2	D[2]	B	Bus	I	---	External bus
153	AN0_1/D1/P0_1	D[1]	B	Bus	I	---	External bus
154	AN0_0/D0/P0_0	D[0]	B	Bus	I	---	External bus
155	IIO0_7/N_RTS6/ N_CTS6/N_SS6/ AN15_7/P15_7	SVID_DET	I	H act	I	---	S-video detect
156	IIO0_6/CLK6/ AN15_6/P15_6	HP_N_DET	I	L act	O	Low	Headphone detection
157	IIO0_5/RXD6/SCL6/ STXD6/AN15_5/ P15_5	EX1_N_CS	O	L act	O	Low	Expansion IO 1 chip select

Pin No.	Port Name	Function Name	Related Power Supply				Detail of Function
			ON		OFF		
			I/O	Logic	I/O	Logic	
158	IIO0_4/TXD6/SDA6/ SRXD6/AN15_4/ P15_4	EX1_N_RST	O	L act	O	Low	Expansion IO 1 reset
159	IIO0_3/N_RTS7/N_ CTS7/AN15_3/P15_3	AD_SEL_A	O		O	Low	AD select A
160	IIO0_2/RXD7/ AN15_2/P15_2	AD_SEL_B	O		O	Low	AD select B
161	IIO0_1/CLK7/ AN15_1/P15_1	IR_OUT	O	Data	O	Low	Remote control cord output
162	VSS	VSS					---
163	IIO0_0/TXD7/ AN15_0/P15_0	AD_SEL_C	O		O	Low	AD select C
164	VCC	VCC					---
165	KI3/AN_7/P10_7	+3.3S_PON	O	H act	O	Low	+3.3S power supply
166	KI2/AN_6/P10_6	AD2_COM	I	A/D	O	Low	AD select 2 COM input
167	KI1/AN_5/P10_5	AD1_COM	I	A/D	O	Low	AD selector 1 COM input
168	KI0/AN_4/P10_4	DEST	I	A/D	O	Low	Destination distinction
169	AN_3/P10_3	MODEL	I	A/D	O	Low	Model distinction
170	AN_2/P10_2	KY_AD2	I	A/D	O	Low	Key 2
171	AN_1/P10_1	KY_AD1	I	A/D	O	Low	Key 1
172	AVSS	AVSS					---
173	AN_0/P10_0	TUN_N_RST	O	L act	O	Low	Tuner reset
		HDR_N_RST	O	L act	O	Low	HD Radio reset (U model)
174	VREF	VREF					---
175	AVCC	AVCC					---
176	STXD4/SCL4/RXD4/ ADTRG/P9_7	TUN_SCL	O	Data	O	Low	Tuner I2C clock
		HDR_MISO	I	Data	O	Low	HD Radio reception data (U model)

Key detection for A/D port
Key input (A/D) pull-up resistance 10 k-ohms

Ohm	0	+ 0.82 k	+ 0.82 k	+ 1.0 k	+ 1.5 k	+ 1.5 k	+ 1.8 k	+ 2.7 k
V	0 – 0.125	0.125 – 0.358	0.358 – 0.577	0.577 – 0.828	0.828 – 1.078	1.078 – 1.299	1.299 – 1.535	1.535 – 1.777
A/D conversion value (3.3 V=255)	0 – 9	10 – 27	28 – 44	45 – 63	64 – 83	84 – 100	101 – 118	119 – 137
KY_AD1 (139 pin of the microprocessor)	SCENE 4	SCENE 3	SCENE 2	SCENE 1	ZONE2 ON/OFF	ZONE3 ON/OFF	ZONE4 ON/OFF	MAIN ZONE ⏻

Ohm	0	+ 0.82 k	+ 0.82 k	+ 1.0 k	+ 1.5 k	+ 1.5 k	+ 1.8 k	+ 2.7 k	+ 3.3 k	+ 4.7 k	+ 6.8 k	+ 12.0 k	+ 22.0 k
V	0 – 0.125	0.125 – 0.358	0.358 – 0.577	0.577 – 0.828	0.828-1.078	1.078 – 1.299	1.299 – 1.535	1.535 – 1.777	1.777 – 2.010	2.010 – 2.241	2.241 – 2.476	2.476 – 2.709	2.709 – 2.940
A/D conversion value (3.3 V=255)	0 – 9	10 – 27	28 – 44	45 – 63	64-83	84 – 100	101 – 118	119 – 137	138 – 155	156 – 173	174 – 191	192 – 209	210 – 227
KY_AD2 (138 pin of the microprocessor)	STRAIGHT	TONE/ BALANCE	OPTION	△	ON SCREEN	<	ENTER	>	PROGRAM <	PROGRAM >	DISPLAY	▽	RETURN

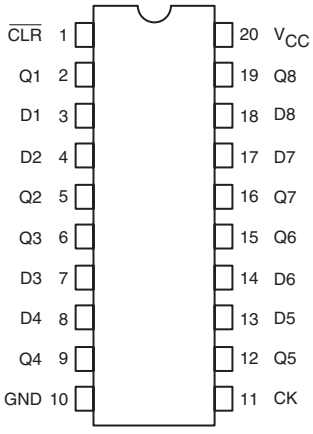
Ohm	0	+ 0.82 k	+ 0.82 k	+ 1.0 k	+ 1.5 k	+ 1.5 k	+ 1.8 k	+ 2.7 k	+ 3.3 k	+ 4.7 k
V	0 – 0.125	0.125 – 0.358	0.358 – 0.577	0.577 – 0.828	0.828 – 1.078	1.078 – 1.299	1.299 – 1.535	1.535 – 1.777	1.777 – 2.010	2.010 – 2.241
A/D conversion value (3.3 V=255)	0 – 9	10 – 27	28 – 44	45 – 63	64 – 83	84 – 100	101 – 118	119 – 137	138 – 155	156 – 173
KY_AD3 (14 pin of the IC902)	PRESET >	PRESET <	MEMORY	INFO	ZONE CONTROL	FM	AM	TUNING/CH <<	TUNING/CH >>	PURE DIRECT

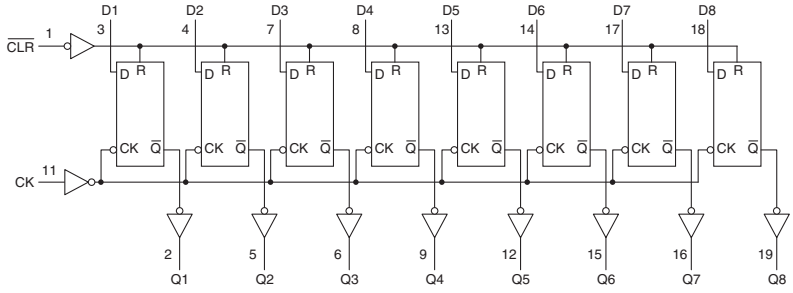
Destination detection for AD port
Pull-up resistance 10 k-ohms

Destination	J	U	C	R	T	K	A	B, G, F	L
A/D conversion value (3.3 V=255)	0 – 12	13 – 39	40 – 67	68 – 92	93 – 115	116 – 140	141 – 169	199 – 221	222 – 244

- **Microprocessor extended port**

IC84, 85: TC74VHC273FT (DIGITAL1 P.C.B.)
Octal D-type flip-flop with clear





Inputs			Output	Function
$\overline{CLR}$	D	CK	Q	
L	X	X	L	Clear
H	L	↑	L	–
H	H	↑	H	–
H	X	↓	Q_n	No Change

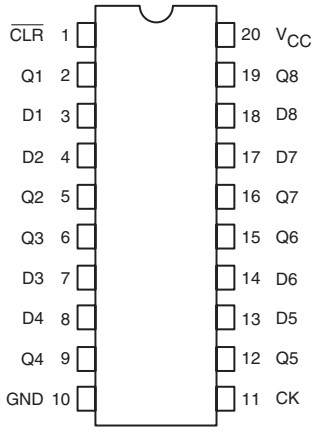
IC84

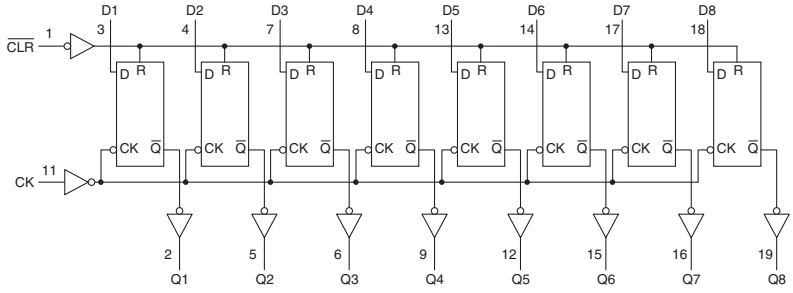
Pin No.	R32C external bus data	Function Name	Related Power Supply				Detail of Function
			ON		OFF		
			I/O	Logic	I/O	Logic	
2	D[8]	HDMI_PON	O	H act	O	Low	HDMI power supply (Necessary for DSP, AVIDEO drive)
5	D[9]	HRX_N_RST	O	L act	O	Low	HDMI RX reset
6	D[10]	HTX1_N_RST	O	L act	O	Low	HDMI TX reset
9	D[11]	HTX2_N_RST	O	L act	O	Low	HDMI TX2 reset
12	D[12]	DAC_N_CS_SW	O	L act	O	Low	DAC chip select SW
15	D[13]	DAC_N_CS_FP	O	L act	O	Low	DAC chip select Front Presence
16	D[14]	DAC_N_RST_SB_FP	O	L act	O	Low	DAC reset Surr B/Front Presence
19	D[15]	DAC_MUTE_RP	O	H act	O	Low	DAC mute Rear Presence

IC85

Pin No.	R32C external bus data	Function Name	Related Power Supply				Detail of Function
			ON		OFF		
			I/O	Logic	I/O	Logic	
2	D[0]	HEQ_N_RST	O	L act	O	Low	HDMI switcher reset
5	D[1]	VDEC_N_RST	O	L act	O	Low	Video decoder reset
6	D[2]	USB_OC_FLG	O	H act	O	Low	USB overcurrent detection flag R32C to BF
9	D[3]	DAC_N_RST	O	L act	O	Low	DAC reset C/SR/SW
12	D[4]	F_HEQ_CE	O	H act	O	Low	Front HDMI EQ chip enable
15	D[5]	VID_PON	O	H act	O	Low	Video power supply
16	D[6]	+3.3D_PON	O	H act	O	Low	OR of HDMI_PON, DSP_PON, NET_USB_PON
19	D[7]	PRY	O	H act	O	Low	Power relay

IC86, 87: TC74VHC273FT (DIGITAL1 P.C.B.)
Octal D-type flip-flop with clear





Inputs			Output	Function
$\overline{CLR}$	D	CK	Q	
L	X	X	L	Clear
H	L	↑	L	–
H	H	↑	H	–
H	X	↓	Q_n	No Change

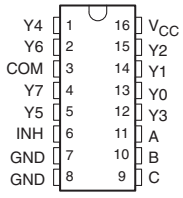
IC86

Pin No.	R32C external bus data	Function Name	Related Power Supply				Detail of Function
			ON		OFF		
			I/O	Logic	I/O	Logic	
2	D[8]	MONO_Z2	O	H act	O	Low	Zone2 stereo/mono output switch
5	D[9]	MONO_Z3	O	H act	O	Low	Zone3 stereo/mono output switch
6	D[10]	EX2_N_RST	O	L act	O	Low	Reset of expansion IO2
9	D[11]	EX2_N_CS	O	H act	O	Low	Chip select of expansion IO2
12	D[12]	–	O	L act	O	Low	No used
15	D[13]	–	O	L act	O	Low	No used
16	D[14]	DAC_MUTE_SW	O	H act	O	Low	DAC mute SW
19	D[15]	DAC_MUTE_FP	O	H act	O	Low	DAC mute Front Presence

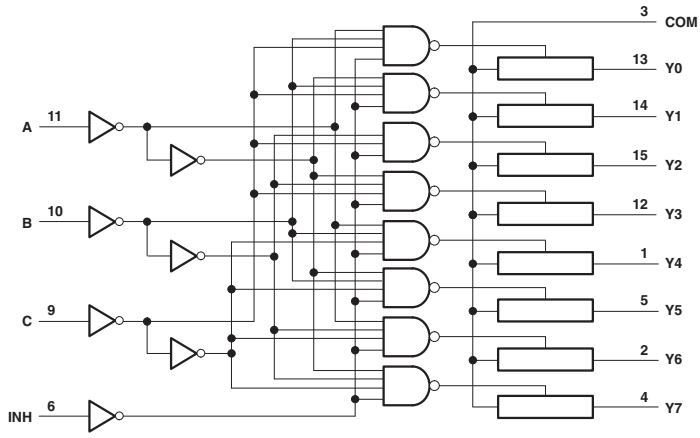
IC87

Pin No.	R32C external bus data	Function Name	Related Power Supply				Detail of Function
			ON		OFF		
			I/O	Logic	I/O	Logic	
2	D[0]	SCR_N_RST	O	L act	O	Low	Reset of scaler (VHD1900)
5	D[1]	SCR_PON	O	H act	O	Low	Scaler (VHD1900) power supply control (No used: Available for power supply control use of AVIDEO)
6	D[2]	FLP_PON	O	H act	O	Low	FL driver VH and filament power supply control
9	D[3]	DAC_N_RST	O	L act	O	Low	DAC Reset C/SR/SB/SW
12	D[4]	DAC_N_RST_F	O	L act	O	Low	DAC Reset Front
15	D[5]	PLL_ON	O	H act	O	Low	Ultra low jitter PLL (CS2300) control
16	D[6]	DSP2_N_RST	O	L act	O	Low	Reset of DSP2
19	D[7]	VOL3_CS	O	L act	O	Low	VOL3 (NJW1194V, NJU7313AM) chip select

IC89, 90: SN74LV4051APWR (DIGITAL1 P.C.B.)
8-channel analog multiplexers/demultiplexers



INPUTS				ON CHANNEL
INH	C	B	A	
L	L	L	L	Y0
L	L	L	H	Y1
L	L	H	L	Y2
L	L	H	H	Y3
L	H	L	L	Y4
L	H	L	H	Y5
L	H	H	L	Y6
L	H	H	H	Y7
H	X	X	X	None



IC89

Pin No.	Port Name	Function Name	Related Power Supply				Detail of Function
			ON		OFF		
			I/O	Logic	I/O	Logic	
1	Y4	PS2_PRT	I	A/D	I	---	Power supply protection 2
2	Y6	PS1_PRT	I	A/D	I	---	Power supply protection 1
4	Y7	AMP_OLV	I	A/D	I	---	Amplifier output level detection
5	Y5	DC_PRT	I	A/D	I	---	DC protection
12	Y3	THM1	I	A/D	I	---	Temperature detection 1
13	Y0	DK1_ID	I	A/D	I	---	Dock ID detection
14	Y1	L3_DET	I	A/D	I	---	D terminal L3 detection
15	Y2	MODE	I	A/D	I	---	Special mode distinction

IC90

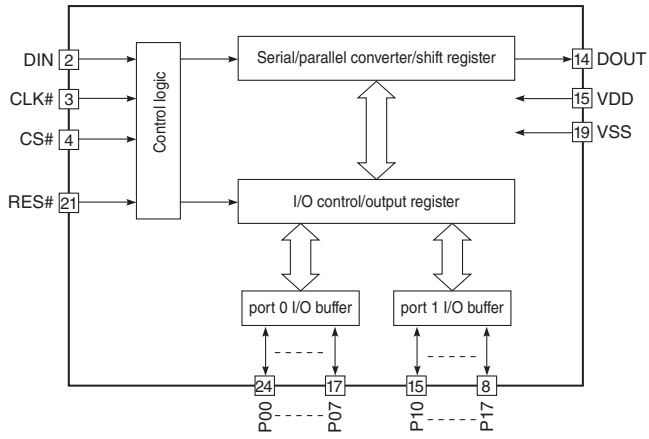
Pin No.	Port Name	Function Name	Related Power Supply				Detail of Function
			ON		OFF		
			I/O	Logic	I/O	Logic	
1	Y4	THM2	I	A/D	I	---	Temperature detection 2
2	Y6	THM3	I	A/D	I	---	Temperature detection 3 (C model)
4	Y7	THM4	I	A/D	I	---	Temperature detection 4 (C model)
5	Y5	KY_AD3	I	A/D	I	---	Key 3
12	Y3	–	I	A/D	I	---	No used
13	Y0	–	I	A/D	I	---	No used
14	Y1	–	I	A/D	I	---	No used
15	Y2	–	I	A/D	I	---	No used

DOCK detection for AD port
Pull-up resistance 10 k-ohms

DOCK type (DKID 13 pin)	Bluetooth (YBA-10)	Wireless iPod (YID-W10)	iPod		No connected
			(YDS-10/11/12(B*))	(YDS-12(A*))	
A/D value (3.3 V=255)	5 – 25	85 – 100	120 – 140	150 – 170	255

* Mode switch setting of the YDS-12

IC182, IC306 : LC709004A-TLM-E (VIDEO P.C.B.)
I/O-expander for microcontroller



IC182

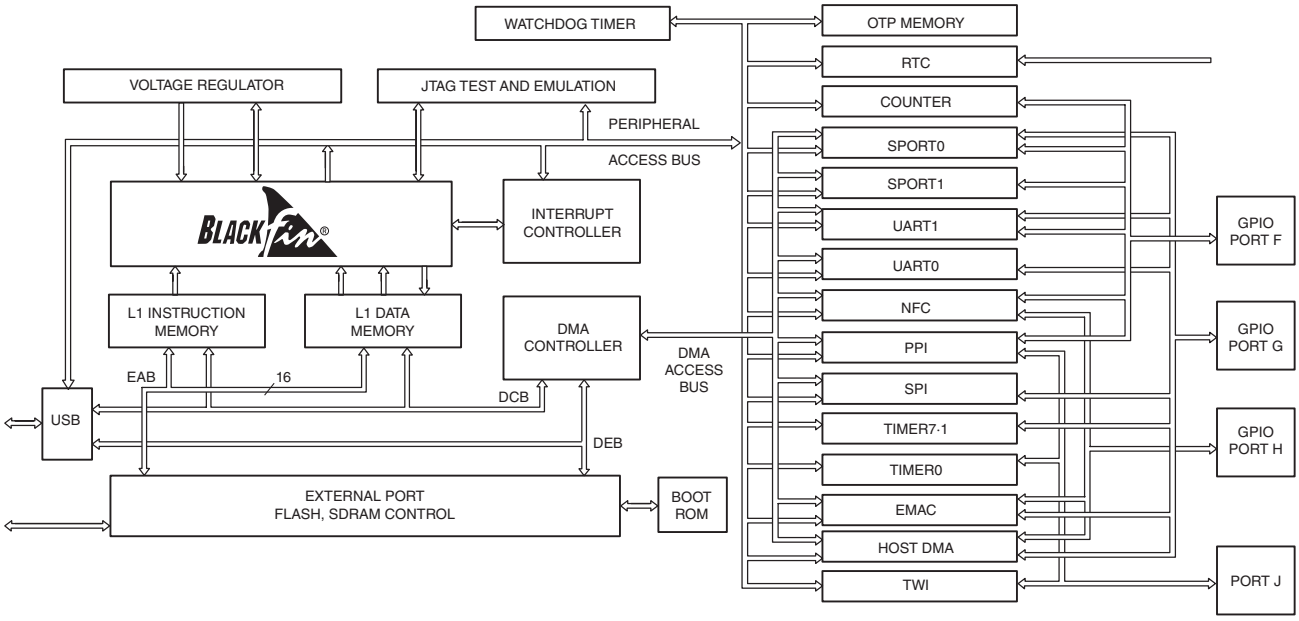
Pin No.	Port Name	Function Name	Related Power Supply				Detail of Function
			ON		OFF		
			I/O	Logic	I/O	Logic	
8	P17	–	–	–	O	Low	No used
9	P16	–	–	–	O	Low	No used
10	P15	–	–	–	O	Low	No used
11	P14	–	–	–	O	Low	No used
12	P13	AMP_POFF	O	H act	O	Low	Reserve (Power amplifier off for preamp mode)
13	P12	PRY2	O	H act	O	Low	Power relay (Z71, Reserve at the time of the toroidal correspondence)
14	P11	–	–	–	O	Low	No used
15	P10	PA_B_RY1	O	H : B = Low	O	Low	Power amplifier B power supply control 1
17	P07	–	–	–	O	Low	No used
18	P06	SPRY_F_RP_CTRL	O	H act	O	Low	SP relay Front –> SP2
19	P05	SPRY_ZRP_CTRL	O	H act	O	Low	SP relay Surround Back –> SP2
20	P04	SPRY_ZFP_CTRL	O	H act	O	Low	SP relay Front Presence –> SP1
21	P03	SPRY_SB_CTRL	O	H act	O	Low	SP relay surround back
22	P02	SPRY_SR_CTRL	O	H act	O	Low	SP relay surround
23	P01	SPRY_C_CTRL	O	H act	O	Low	SP relay center
24	P00	SPRY_F_CTRL	O	H act	O	Low	SP relay front

IC306

Pin No.	Port Name	Function Name	Related Power Supply				Detail of Function
			ON		OFF		
			I/O	Logic	I/O	Logic	
8	P17	–	O	Low	O	Low	No used
9	P16	–	O	Low	O	Low	No used
10	P15	–	O	Low	O	Low	No used
11	P14	DC_TRG2	O	H act	O	Low	Control out 2
12	P13	–	O	Low	O	Low	No used
13	P12	DC_TRG1	O	H act	O	Low	Control out 1
14	P11	VO_SEL2	O	Low	O	Low	MON output select of Y/C
15	P10	VO_SEL1	O	Low	O	Low	MON output select of Y/C
17	P07	–	O	Low	O	Low	No used
18	P06	VID_SEL1	O		O	Low	Input select of Y/C
19	P05	VID_SEL2	O		O	Low	Input select of Y/C
20	P04	VID_SEL3	O		O	Low	Input select of Y/C
21	P03	V_N_FMUTE	O		O	Low	Video full mute
22	P02	VZ_SEL3	O		O	Low	Zone2 select of Y/C
23	P01	VZ_SEL2	O		O	Low	Zone2 select of Y/C
24	P00	VZ_SEL1	O		O	Low	Zone2 select of Y/C

IC901: ADSST-DR-11Z (DIGITAL1 P.C.B.)
Network microprocessor

*** No replacement part available.**



Pin No.		Port Name	Function Name	ON		Detail of Function
				I/O	Logic	
1	A1	GND	GND			
2	A2	PF9/PPI_D9/ RSCLK1/%SPISEL6%	DBG_LED1	B	Data	Debug input/output port1 (DIP_SW1 input/LED1 output)
3	A3	PF11/PPI_D11/TFS1/CZM	BF_WCK1	I	Clock	I2S word clock input
4	A4	SCL	BF_I2C_SCL	O	Clock	EEPROM / VideoENC / Apple_Coprocessor / Clock I2C data
5	A5	PF13/PPI_D13/ TSCLK1/%SPISEL3%/CUD	BF_BCK1	I	Clock	I2S Bit clock input
6	A6	PF15/PPI_D15/DR1SEC/UAR-T1RX/TACI3	---			
7	A7	PH0/ND_D0/MIICRS/RMIICRSDV/ HOST_D0	RMII_CRSDV	I	Data	PHY: RMII carrier sence/DataValid
8	A8	PH2/ND_D2/MDIO/HOST_D2	PHY_MDIO	B	Data	PHY: Management channel clock
9	A9	PH4/ND_D4/MIITXCLK/RMII_REF-CLK/HOST_D4	RMII_REFCLK	I	Clock	PHY: RMII reference clock (50MHz)
10	A10	XTAL				23.04MHz crystal
11	A11	CLKIN				23.04MHz crystal
12	A12	PH8/%SPISEL4%/ERXD1/HOST_ D8/TACLK2	RMII_RXD1	I	Data	PHY: RMII RXD1
13	A13	PH10/%ND_CE%/ERXD2/HOST_ D10	PHY_N_FDX	I	Data	PHY: PHY_NWAYEN
14	A14	RTXI		I	Clock	
15	A15	RTXO		O	Clock	
16	A16	VDDRTC				
17	A17	GND				
18	A18	USB_XO		O	Clock	
19	A19	USB_XI		I	Clock	24MHzUSB clock input
20	A20	GND				
21	B1	PF7/PPI_D7/DR0SEC/ND_D7A/ TACI1	USB_FSSEL	O	Data	I2S (USB) FS select
22	B2	PF8/PPI_D8/DR1PRI	DBG_LED0	B	Data	Debug input/output port0 (DIP_SW0 input/LED0 output)
23	B3	PF10/PPI_D10/RFS1/%SPISEL7%	PLD_N_RST	O	L act	PLD reset
24	B4	SDA	BF_I2C_SDA	B	Data	I2C data (EEPROM / Apple_Coprocessor / Clock)
25	B5	PF12/PPI_D12/ DT1PRI/%SPISEL2%/CDG	BF_SDO1	O	Data	I2S1 data output
26	B6	PF14/PPI_D14/DT1SEC/UART1TX	APPLE_N_RST	O	L act	Apple certification chip reset (L: reset)
27	B7	PH1/ND_D1/ERXER/HOST_D1	RMII_RXER	I	Data	PHY: RMII receive error
28	B8	PH3/ND_D3/ETXEN/HOST_D3	RMII_TXEN	O	Clock	PHY: RMII TX enable

Pin No.		Port Name	Function Name	ON		Detail of Function
				I/O	Logic	
29	B9	PH5/ND_D5/ETXD0/HOST_D5	RMII_TXD0	O	Data	PHY: RMII TXD0
30	B10	PH6/ND_D6/ERXD0/HOST_D6	RMII_RXD0	I	Data	PHY: RMII RXD0
31	B11	PH7/ND_D7/ETXD1/HOST_D7	RMII_TXD1	O	Data	PHY: RMII TXD1
32	B12	PH9/%SPISEL5%/ETXD2/HOST_D9/TACLK3	SPI_N_ON	O	Data	R32C to/from Blackfin SPI_I/F switch control (L: active, H: off)
33	B13	PH11/%ND_WE%/ETXD3/HOST_D11	PHY_N_100M	O	Data	PHY_SPEED
34	B14	PH12/%ND_RE%/ERXD3/HOST_D12	PHY_N_RST	O	H act	PHY Rset (L: reset)
35	B15	PH13/%ND_BUSY%/ERXCLK/HOST_D13	USB_PWR	O	H act	USB vbus power Control (H: power on)
36	B16	PH14/ND_CLE/ERXDV/HOST_D14	BF_MT	O	H act	Mute output to R32C
37	B17	PH15/ND_ALE/COL/HOST_D15	USB_OC_FLG	I	H act	USB vbus over current flag (R32C to BF)
38	B18	/RESET	BF_N_RST	I	Lact	CPU reset
39	B19	/NMI				
40	B20	GND				
41	C1	PF5/PPI_D5/TSCLK0/ND_D5A/TACLK1	BF_BCK0	I	Clock	I2S0 BCK input
42	C2	PF6/PPI_D6/DT0SEC/ND_D6A/TACI0	USB_MSEL	O	Data	I2S (USB) master clock select
43	C19	CLKBUF	(USB_REFCLK)			CPU clock buffered output
44	C20	USB_ID	USB_ID	I	Data	USB ID
45	D1	PF3/PPI_D3/DT0PRI/ND_D3A	BF_SDO0	O	Data	I2S0 data output
46	D2	PF4/PPI_D4/TFS0/ND_D4A/TACLK0	BF_WCK0	I	Clock	I2S0 WCK input
47	D19	VDDUSB				
48	D20	USB_RSET	---			
49	E1	PF1/PPI_D1/RFS0/ND_D1A	NET_FSSEL	O	Data	I2S (NET) FS select
50	E2	PF2/PPI_D2/RSCLK0/ND_D2A	R32C_N_INT	I	L act	Interrupt input from R32C
51	E19	USB_VBUS	USB_VBUS	I	-	USB_VBUS
52	E20	USB_DP	USB_DP	B	Data	USB Data D+
53	F1	PF0/PPI_D0/DR0PRI/ND_D0A	NET_MSEL	O	Data	I2S (NET) master clock select
54	F2	PPI_FS1/TMR0	---			
55	F19	VRSEL/VDDEXT				
56	F20	USB_DM	USB_DM	B	Data	USB data D-
57	G1	PG15/TFS0A/MII PHYINT/RMII MDINT/HOST_CE	RMII_MDINT			RMII management
58	G2	PPI_CLK/TMRCLK				
59	G7	VDDEXT				
60	G8	VDDEXT				
61	G9	VDDEXT				
62	G10	VDDEXT				
63	G11	VDDEXT				
64	G12	VDDINT				
65	G13	VDDINT				
66	G14	VDDINT				
67	G19	SS//PG				
68	G20	VDDUSB				
69	H1	PG13/DMAR0/UART1RXA/HOST_ADDR/TACI2	NCPU_MOSI	I	Data	UART input R32C to Blackfin
70	H2	PG14/TSCLK0A1/MDC/%HOST_RD%	PHY_MDC			PHY MDC
71	H7	VDDEXT				
72	H8	VDDEXT				
73	H9	GND				
74	H10	GND				
75	H11	GND				
76	H12	GND				
77	H13	GND				
78	H14	VDDINT				
79	H19	USB_VREF		O	-	
80	H20	VROUT/EXT_WAKE1	VROUT	O	PWM	
81	J1	PG11/TMR7/%HOST_WR%	NCPU_N_INT	O	L act	Interrupt to BF to R32C
82	J2	PG12/DMAR1/UART1TXA/HOST_ACK	NCPU_MISO	O	Data	UART output Blackfin to R32C
83	J7	VDDEXT				
84	J8	VDDEXT				
85	J9	GND				

Pin No.		Port Name	Function Name	ON		Detail of Function
				I/O	Logic	
86	J10	GND				
87	J11	GND				
88	J12	GND				
89	J13	GND				
90	J14	VDDINT				
91	J19	/AMS0	---			
92	J20	EXT_WAKE0		O	Data	Wake up indication 0
93	K1	PG9/TMR5/RSCLK0A/TACI5	NCPU_PIC_MISO	O	L act	Buffer overflow flag of FPGA
94	K2	PG10/TMR6/TSCLK0A/TACI6	MT_DAC_Z	O	H act	ZONE DAC mute
95	K7	VDDEXT				
96	K8	VDDEXT				
97	K9	GND				
98	K10	GND				
99	K11	GND				
100	K12	GND				
101	K13	GND				
102	K14	VDDINT				
103	K19	/AMS1	---			
104	K20	CLKOUT	BF_CLK	O	Clock	SDRAM clock
105	L1	PG7/TMR3/DR0PRIA/UART0TX	DBG_MOSI	O	Data	UART Tx for Debug
106	L2	PG8/TMR4/RFS0A/UART0RX/ TACI4	DBG_MISO	I	Data	UART Rx for Debug
107	L7	VDDEXT				
108	L8	VDDMEM				
109	L9	GND				
110	L10	GND				
111	L11	GND				
112	L12	GND				
113	L13	GND				
114	L14	VDDINT				
115	L19	VPPOTP				
116	L20	/AMS3	---			
117	M1	PG5/TMR1/PPI_FS2	---	O	L act	
118	M2	PG6/DT0PRIA/TMR2/PPI_FS3	APPLE_I2C_ON	O	H act	APPLE I2C line switch control (H: connect, L: disconnect)
119	M7	VDDMEM				
120	M8	VDDMEM				
121	M9	GND				
122	M10	GND				
123	M11	GND				
124	M12	GND				
125	M13	GND				
126	M14	VDDINT				
127	M19	/AMS2	---			
128	M20	/ARE	BF_N_ARE	O	L act	EBIU read enable
129	N1	PG3/MISO/DR0SECA	BF_SPI_MISO	I	Data	
130	N2	PG4/MOSI/DT0SECA	BF_SPI_MOSI	O	Data	
131	N7	VDDMEM				
132	N8	VDDMEM				
133	N9	GND				
134	N10	GND				
135	N11	GND				
136	N12	GND				
137	N13	GND				
138	N14	VDDINT				
139	N19	/AWE	BF_N_WR	O	L act	EBIU write enable
140	N20	/AOE	---	O	L act	
141	P1	PG1/SPISS/SPISEL1	SFLASH_N_CS	O	L act	SPI flash memory chip select output (L: select)
142	P2	PG2/SCK	BF_SPI_SCK	O	Clock	SPI clock
143	P7	VDDMEM				
144	P8	VDDMEM				
145	P9	VDDMEM				
146	P10	VDDMEM				
147	P11	VDDMEM				
148	P12	VDDINT				
149	P13	VDDINT				
150	P14	VDDINT				
151	P19	ARDY	---	I	H act	
152	P20	SCKE	BF_SCKE	O	H act	SDRAM CKE

Pin No.		Port Name	Function Name	ON		Detail of Function
				I/O	Logic	
153	R1	TDI	BF_JTAG_TDI	I	Data	ICE Debug TDI
154	R2	PG0/HWAIT	BF_JTAG_N_INT	I	Inter-rupt	
155	R19	/SMS	BF_N_SMS	O	L act	SDRAM chip select
156	R20	VDDOTP				
157	T1	TDO	BF_JTAG_TDO	O	Data	ICE Debug TDO
158	T2	/EMU	BF_JTAG_N_EMU	O	Data	ICE Debug /EMU
159	T19	/SRAS	BF_N_SRAS	O	L act	SDRAM /RAS
160	T20	/SWE	BF_N_SWE	O	L act	SDRAM /WE
161	U1	TRST	BF_JTAG_N_TRST	I	L act	ICE Debug /TRST
162	U2	TMS	BF_JTAG_TMS	O	Data	ICE Debug TMS
163	U19	SA10	BF_SA10	O	Data	SDRAM A10
164	U20	/SCAS	BF_N_SCAS	O	L act	SDRAM /CAS
165	V1	DATA15	BF_D[15]	B	Data	Data bus bit 15
166	V2	TCK	BF_JTAG_TCK	I	Clock	
167	V19	/ABE0/SDQM0	BF_SDQM0	O	H act	SDRAM DQM0
168	V20	/ABE1/SDQM1	BF_SDQM1	O	H act	SDRAM DQM1
169	W1	DATA14	BF_D[14]	B	Data	Data bus bit 14
170	W2	DATA13	BF_D[13]	B	Data	Data bus bit 13
171	W3	DATA11	BF_D[11]	B	Data	Data bus bit 11
172	W4	DATA9	BF_D[9]	B	Data	Data bus bit 9
173	W5	DATA7	BF_D[7]	B	Data	Data bus bit 7
174	W6	DATA5	BF_D[5]	B	Data	Data bus bit 5
175	W7	DATA3	BF_D[3]	B	Data	Data bus bit 3
176	W8	DATA1	BF_D[1]	B	Data	Data bus bit 1
177	W9	BMODE3	BMODE3			Boot mode select 3
178	W10	BMODE1	BMODE1			Boot mode select 1
179	W11	ADDR18	BF_A[18]	O	Data	Address bus bit 18
180	W12	ADDR16	BF_A[16]	O	Data	Address bus bit 16
181	W13	ADDR14	BF_A[14]	O	Data	Address bus bit 14
182	W14	ADDR12	BF_A[12]	O	Data	Address bus bit 12
183	W15	ADDR10	BF_A[10]	O	Data	Address bus bit 10
184	W16	ADDR8	BF_A[8]	O	Data	Address bus bit 8
185	W17	ADDR6	BF_A[6]	O	Data	Address bus bit 6
186	W18	ADDR4	BF_A[4]	O	Data	Address bus bit 4
187	W19	ADDR2	BF_A[2]	O	Data	Address bus bit 2
188	W20	ADDR1	BF_A[1]	O	Data	Address bus bit 1
189	Y1	GND				
190	Y2	DATA12	BF_D[12]	B	Data	Data bus bit 12
191	Y3	DATA10	BF_D[10]	B	Data	Data bus bit 10
192	Y4	DATA8	BF_D[8]	B	Data	Data bus bit 8
193	Y5	DATA6	BF_D[6]	B	Data	Data bus bit 6
194	Y6	DATA4	BF_D[4]	B	Data	Data bus bit 4
195	Y7	DATA2	BF_D[2]	B	Data	Data bus bit 2
196	Y8	DATA0	BF_D[0]	B	Data	Data bus bit 0
197	Y9	BMODE2	GND			
198	Y10	BMODE0	+3.3V			
199	Y11	ADDR19	BF_A[19]	O	Data	Address bus bit 19
200	Y12	ADDR17	---			
201	Y13	ADDR15	---			
202	Y14	ADDR13	BF_A[13]	O	Data	Address bus bit 13
203	Y15	ADDR11	---			
204	Y16	ADDR9	BF_A[9]	O	Data	Address bus bit 9
205	Y17	ADDR7	BF_A[7]	O	Data	Address bus bit 7
206	Y18	ADDR5	BF_A[5]	O	Data	Address bus bit 5
207	Y19	ADDR3	BF_A[3]	O	Data	Address bus bit 3
208	Y20	GND				

MEMO